IN THE CLAIMS:

Claims 1-11 (Cancelled)

12. (Currently amended) A multilayer structure incorporating γ-aluminum oxide ~~deposited according to claim 1~~ having substantially no re-growth of interfacial oxide, wherein no hydroxyl absorption is observed in said γ-aluminum oxide by FTIR.

13. (Currently amended) A multicomponent film incorporating γ-aluminum ~~oxide deposited according to claim 1.~~ having substantially no re-growth of interfacial oxide, wherein no hydroxyl absorption is observed in said γ-aluminum oxide by FTIR.

14. (Currently amended) An electronic device that contains γ-aluminum oxide ~~deposited according to claim 1.~~ having substantially no re-growth of interfacial oxide, wherein no hydroxyl absorption is observed in said γ-aluminum oxide by FTIR.

15. (Original) The electronic device of claim 14 selected from the group consisting of a transistor, capacitor, diode, resistor, switch, light emitting diode, laser, wiring structure, and interconnect.

16. (Currently amended) A capacitor structure fabricated by sequentially depositing a bottom electrode layer, a dielectric layer and a top electrode layer on a base structure wherein the dielectric layer incorporates γ-aluminum oxide ~~deposited according to claim 1.~~ having substantially no re-growth of interfacial oxide and no hydroxyl absorption observed in said γ-aluminum oxide by FTIR.

17. (Original) The capacitor structure of claim 16 wherein the capacitor structure is selected from the group consisting of stack capacitors and trench capacitors.

18. (Original) The capacitor structure of claim 16 further comprising depositing a dielectric buffer layer over the capacitor structure.

19. (Currently amended) The capacitor structure of claim 18 wherein the optional dielectric buffer layer is selected from the group consisting of γ-aluminum oxide and a multilayer structure with γ-aluminum oxide and any insulating material wherein said γ-aluminum oxide ~~is deposited according to claim 1.~~ has substantially no re-growth of interfacial oxide and no hydroxyl absorption is observed in said γ-aluminum oxide by FTIR.

20. (Currently Amended) The capacitor structure of claim 16 wherein the capacitor structure is connected to underlying circuitry via a plug and an optional conductive barrier.

21. (Original) The capacitor structure of claim 20 wherein the plug material is selected from the group consisting of polysilicon, W, Mo, Ti, Cr, Cu, and doped or undoped alloys, mixtures or multilayers thereof.

22. (Original) The structure of claim 20 wherein the conductive barrier is selected from the group consisting of TaN, TaSiN, TiAlN, TiSiN, TaSiN, TaWN, TiWN, TaSiN, TaAlN, NbN, ZrN, TaTiN, TiSiN, TiAlN, IrO_2, SiC, TiPt, TiNPt, TiAlN-Pt, Ru, RuO_2, RuPt, RuO_2, WSi, Ti, TiSi, doped and undoped polysilicon, Al, Pd, Ir, IrO_x, Os, OsO_x, MoSi, TiSi, ReO_2, and doped or undoped alloys, mixtures or multilayers thereof.

23. (Original) The structure of claim 16 wherein the bottom electrode is selected from the group consisting of conductive materials, polysilicon, Ni, Pd, Pt, Cu, Ag, Au, Ru, Ir, Rh, IrO_x, RuO_x, TaN, TaSiN, Ta, $SrRuO_3$, $LaSrCoO_3$, and doped or undoped alloys, mixtures or multilayers, thereof.

24. (Currently amended) The structure of claim 16 wherein the dielectric material is selected from the group consisting of γ-aluminum oxide and a multilayer structure of γ-aluminum oxide and any insulating material.

25. (Currently amended) The structure of claim 16 wherein the top electrode is selected from the group consisting of polysilicon, Ni, Pd, Pt, Cu, Ag, Au, Ru, Ir, Rh,IrO_x, RuO_x, TaN, TaSiN, Ta, $SrRuO_3$, $LaSrCoO_3$, and doped or undoped alloys, mixtures or multilayers thereof.

26. (Currently amended) A wiring structure formed by etching trenches and vias into a dielectric layer, patterning the metallization layer, depositing an optional barrier material, and depositing a wiring material, wherein the dielectric layer and/or the optional barrier material incorporate γ-aluminum oxide ~~deposited according to claim 1.~~having substantially no re-growth of interfacial oxide and no hydroxyl absorption observed in said γ-aluminum oxide by FTIR.

27. (Currently amended) The structure of claim 26 wherein the dielectric layer is selected from the group consisting of γ-aluminum oxide and multilayers of γ-aluminum oxide and SiO_2, SiO_xN_y, Si_3N_4, phosphosilicate glass, metal oxides, doped or undoped alloys, mixtures or multilayers, thereof, wherein said γ-aluminum oxide ~~is deposited according to claim 1.~~ has substantially no re-growth of interfacial oxide and no hydroxyl absorption observed in said γ-aluminum oxide by FTIR.

28. (Currently amended) The structure of claim 26 wherein the optional barrier material is selected from the group consisting of γ-aluminum oxide and doped or undoped alloys, mixtures or multilayers, thereof of γ-aluminum oxide and WN, TiN, TaN, SiO_2, SiO_xN_y, Si_3N_4, phosphosilicate glass, metal oxides, wherein γ-aluminum oxide has substantially no regrowth of interfacial oxide and no hydroxyl absorption observed in said γ-aluminum oxide by FTIR.

29. (Original) The structure of claim 26 wherein the wiring material is selected from the group consisting of polysilicon, Al, W, Mo, Ti, Cr, Cu and doped or undoped alloys, mixtures or multilayers thereof.

30. (Currently amended) A structure comprising a substrate having source and drain regions and a channel region between said source and drain regions; depositing a gate dielectric, aligned to and on top of said channel region; and depositing a gate electrode aligned to and on top of said gate dielectric wherein the gate dielectric incorporates γ-aluminum oxide ~~deposited according to claim 1~~ having substantially no re-growth of interfacial oxide and no hydroxyl absorption observed in said γ-aluminum by FTIR.

31. (Cancelled)

32. (Currently amended) The structure of claim 30 wherein the gate dielectric is selected from the group consisting of aluminum oxide and doped or undoped alloys, mixtures or multilayers of aluminum oxide and SiO_2, SiO_xN_y, Si_3N_4, BaO, SrO, CaO, Ta_2O_5, TiO_2, ZrO_2, HfO_2, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, wherein γ-aluminum oxide ~~is deposited according to claim 1.~~ has substantially no re-growth of interfacial oxide and no hydroxyl absorption observed in said γ-aluminum oxide by FTIR.

33. (Currently amended) The structure of claim 30 wherein the gate dielectric is composed of more than one layer and at least one component of at least one of the layers comprising the gate dielectric is γ-aluminum oxide ~~deposited according to claim 1.~~ having substantially no regrowth of interfacial oxide, wherein no hydroxyl absorption is observed in said γ-aluminum oxide by FTIR.

34. (Currently amended) The structure of claim 30 wherein the multilayer gate dielectric is composed of a lower, middle and optional upper layer wherein at least one layer or one component of a layer of the gate dielectric is γ-aluminum oxide ~~deposited according to claim 1~~ having substantially no re-growth of interfacial oxide and no hydroxyl absorption observed in said γ-aluminum oxide by FTIR.

35. (Original) The structure of claim 34 wherein the lower layer is selected from the group consisting of SiO_2, SiO_xN_y, Si_3N_4, BaO, SrO, CaO, Ta_2O_5, TiO_2, ZrO_2, HfO_2, Al_2O_3, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, and doped or undoped alloys, mixtures or multilayers, thereof.

36. (Original) The structure of claim 34 wherein the middle layer is selected from the group consisting of SiO_2, SiO_xN_y, BaO, SrO, CaO, Si_3N_4, Ta_2O_5, TiO_2, ZrO_2, HfO_2, Al_2O_3, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, and doped or undoped alloys, mixtures or multilayers, thereof.

37. (Original) The structure of claim 34 wherein the upper layer is selected from the group consisting of SiO_2, SiO_xN_y, Si_3N_4, BaO, SrO, CaO, Ta_2O_5, TiO_2, ZrO_2, HfO_2, Al_2O_3, La_2O_3, Y_2O_3, yttrium alumnate, lathnaum alumnate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, and doped or undoped alloys, mixtures or multilayers, thereof.

38. (Original) The structure of claim 30 wherein the gate electrode is selected from the group consisting of polysilicon, Al, Ag, Bi, Cd, Fe, Ga, Hf, In, Mn, Nb, Y, Zr, Ni, Pt, Be, Ir, Te, Re, Rh, W, Mo, Cr, Fe, Pd, Au, Rh, Ti, Cr, Cu, and doped or undoped alloys, mixtures or multilayers, thereof.